

Simple-structured Control for Supercapacitor DC-DC Converters for Grid-connected Applications

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Abstract—The bi-directional DC-DC converter (DDC) is commonly employed for a battery or supercapacitor (BA/SC) to accomplish power management flexibility. Current and voltage control for the DDC is crucial for power management. Focusing on control of the DDC, this paper first proposes a simple order-reduction control method for the first-order system, then applies the proposed control method to current and voltage control of the SC DDC. The effect of the inner current loop on the outer DC bus voltage loop is also analyzed. With the proposed simple order-reduction control method, the dynamic response of the SC DDC is obviously improved, and robustness to the SC voltage variation is achieved. The double-line-frequency ripple is also eliminated through the proposed simple and effective method. Finally, the effectiveness of the developed control algorithm is tested by the experiment.

Index Terms—Battery/supercapacitor, DC-DC converter, order-reduction control, zero-pole cancellation.

I. INTRODUCTION

BATTERY and/or supercapacitor (SC) energy storage devices are regularly and increasingly utilized in energy storage systems [1]–[3], electric vehicles [4]–[6], microgrids [7], [8], and AC/DC hybrid distribution systems [9]. A DC-DC converter (DDC) is typically employed to connect the battery/supercapacitor and the DC connection. Then power conversion and control are accomplished by the DDC. Therefore, control of the DDC is crucial to accomplishing flexible power conversion [10].

Generally, a non-isolated DDC adopts a half-bridge structure to accomplish bi-directional power transmission. Then power control can be accomplished by controlling the fundamental voltage or current of the bi-directional DDC. The

bi-directional DDC generally employs a conventional double-loop control. For instance, the battery or SC typically adopts an inner current loop (ICL) with an outer voltage loop (OVL) as the control structure [1], [2]. Besides, a proportional-integral (PI) controller is the most widely used controller to realize a zero-steady-state-error current and voltage control [2], [11], [12]. The PI controller provides benefits of clear physical meaning, easy parameter design, and straightforward implementation. Consequently, the PI controller receives wide application in control of DDCs. Recently, to improve control performance, lots of advanced control methods are also proposed for the DDC, such as model predictive control [13], [14], sliding-model control [15], [16], optimal control [17], adaptive control [18], [19], robust control [20], intelligent control including fuzzy logic controllers [21], and reinforcement learning [22].

Generally, a fast power response is required for the application of the SC. In this condition, current control is important to achieve a fast-dynamic response, because the current of the SC should track the current reference at a very fast speed. To achieve fast dynamic response (DR), a parallel control structure are proposed [14], [16], [17], [19], [22]. In the parallel control structure, current is used as a state variable to damp the system, where the output voltage is controlled to track the reference, and different advanced design methods have been proposed. These controllers can achieve good DR; however, they are not suitable for SC/battery applications, because current-tracking control is required for charging the SC/battery. For the dual-loop control structure, the model predictive control [13], sliding-mode control [15], and type-II PI controller [21] are applied to the ICL to realize fast DR. While in [15], the adaptive control is employed for the OVL and the linear PI controller is adopted for the inner current loop. These nonlinear controllers in [13]–[22] achieve good performance for control of the DDC. However, these nonlinear controllers usually require greater mathematical understanding, as well as precise models to design the parameters. Moreover, these nonlinear controllers are usually complicated for practical implementation.

In contrast, linear PI controllers are developed simply based on classical control theory. For instance, a standard PI controller is intended to produce 4 kHz bandwidth with a 45° phase margin for inner current regulation in [11]. Nonetheless, because of the zero created by the PI controller, overshoot

Manuscript received November 14, 2021; revised April 13, 2022; accepted May 19, 2022. Date of online publication October 12, 2022; date of current version July 20, 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52007034.

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DOI: 10.17775/CSEEJPES.2021.08480

commonly appears on the current [2]. As stated in [2], the ICL might be modeled as a second-order system (SOS) with an extra zero. In this scenario, the SOS is not beneficial for building the OVL, and the overshoot is also detrimental to the DR. On the other hand, when the SC is applied to a grid-connected system, low-frequency elimination is an important task to address the double-grid-frequency ripple which is caused by unbalanced power of the grid [11], [23], [24]. Compensation of the double-grid-frequency ripple has been well studied. Generally, the elimination of a double-grid-frequency ripple can be achieved by instantaneous power control of the AC side. This method will not be discussed further in this paper. Another method to address the low-frequency ripple (LFR) is advanced control of the DDC [11], [23]. In [23], the DDC is used to generate a 180° phase-shifted second-order ripple to offset the ripple in the DC bus. This method is an open-loop feedforward method and needs to estimate the ripple phase, which is not an easy task. Hence, the authors in [11] designed a closed-loop (CL) control using PI plus a multi-resonant controller to eliminate the low-frequency ripple of the DC bus. Furthermore, this method also leads to the concept of the active capacitor. A similar concept is also proposed in [25] and [26] with enhanced plug-and-play ability. Later, the active capacitor is controlled with infinite capacitance which is called a virtual infinite capacitor [27]. Furthermore, the plug-and-play performance is achieved for the virtual infinite capacitor in [28]. Control is complicated for these active capacitor techniques since multiple resonant controllers or multiple loops are generally needed.

In practice, when the SC is employed by a grid-connected system, which is a common application, the SC can compensate for the low-frequency ripple of the DC bus [29]. Furthermore, if the capacitance of the SC is always large, then voltage fluctuation of the supercapacitor is small. This will be an advantage for the control design. Therefore, this paper will propose a simple control method to achieve excellent performance. The following contributions are achieved:

- 1) a state-space-based (SS-based) control structure for a general first-order system (FOS) is proposed to reduce the control system to be a FOS;
- 2) good DR with zero overshoot and fast settling time is achieved when the proposed control method is applied to current and voltage control for the DDC;
- 3) the double-line-frequency voltage ripple is easily eliminated by a power feedforward.

Finally, the effectiveness of the proposed control approach is experimentally certified.

II. PROPOSED CONTROL FOR FIRST-ORDER SYSTEM

In this section, we first propose a simple control method for the first-order control objective that can be described by

$$\frac{dx_p}{dt} = ax_p + b_1u_c + b_2u_d \quad (1)$$

where x_p is the state variable and the output variable that needs to be controlled, u_c is the control input, u_d is the

disturbance. For the FOS (1), defining the integral controller with the reference x_{pref} as:

$$\frac{dx_c}{dt} = x_{pref} - x_p \quad (2)$$

we can obtain the open-loop system

$$\frac{d}{dt} \begin{bmatrix} x_p \\ x_c \end{bmatrix} = \begin{bmatrix} a & 0 \\ -1 & 0 \end{bmatrix} \begin{bmatrix} x_p \\ x_c \end{bmatrix} + \begin{bmatrix} b_1 \\ 0 \end{bmatrix} u_c + \begin{bmatrix} b_2 \\ 0 \end{bmatrix} u_d + \begin{bmatrix} 0 \\ 1 \end{bmatrix} x_{pref} \quad (3)$$

Then, designing the control law

$$u_c = k_px_p + k_ix_c + k_du_d + k_rx_{pref} \quad (4)$$

The system's CL model is derived as:

$$\frac{d}{dt} \begin{bmatrix} x_p \\ x_c \end{bmatrix} = \begin{bmatrix} a + b_1k_p & b_1k_i \\ -1 & 0 \end{bmatrix} \begin{bmatrix} x_p \\ x_c \end{bmatrix} + \begin{bmatrix} b_2 + b_1k_d \\ 0 \end{bmatrix} u_d + \begin{bmatrix} b_1k_r \\ 1 \end{bmatrix} x_{pref} \quad (5)$$

From this CL model, the transfer functions (TFs) can be computed as:

$$G_{rc}(s) = \frac{x(s)}{x_{pref}(s)} = \frac{b_1k_r(s + k_i/k_r)}{s^2 - (a + b_1k_p)s + b_1k_i}$$

$$G_{dc}(s) = \frac{x(s)}{u_d(s)} = \frac{(b_2 + b_1k_d)s}{s^2 - (a + b_1k_p)s + b_1k_i} \quad (6)$$

Obviously, using the proposed control algorithm, the CL TF $G_{rc}(s)$ includes two poles that are associated with k_p , k_i , and a zero that can be tuned by reference feedforward k_r . The gain of $G_{dc}(s)$ can be tuned by k_d .

To shape the reference-tracking performance, the TF $G_{rc}(s)$ is expressed in a zero-pole form:

$$G_{rc}(s) = \frac{x(s)}{x_{pref}(s)} = \frac{b_1k_r(s + z)}{(s + p_1)(s + p_2)} \quad (7)$$

where $p_1 > 0$, $p_2 > 0$, $z > 0$. Then, it has

$$p_1 + p_2 = -(a + b_1k_p)$$

$$p_1p_2 = b_1k_i \quad (8)$$

and

$$z = k_i/k_r \quad (9)$$

The poles can be determined k_p and k_i , while the location of the zero can be tuned k_r . In addition, k_i also affects the zero. It means the parameters can be designed by placing the zeros and poles. Generally, we set the poles to be a couple of conjugate complex values that have a 0.707 damping ratio, resulting in the best DR. However, the zero usually strengthens the overshoot and oscillations [30]. Furthermore, the proposed control has one configurable zero. Therefore, we will place two real poles, one of which can be canceled by the configurable zero. As a result, the SOS is transformed to a first-order system with another pole determining its DR. This is beneficial for outer DC bus voltage control.

Consequently, once the poles are determined as $p_1 > 0$, $p_2 > 0$, the parameters k_p and k_i can be expressed as:

$$k_p = -\frac{a + p_1 + p_2}{b_1}$$

$$k_i = \frac{p_1 p_2}{b_1} \quad (10)$$

where k_r is configured by $z = p_2$:

$$k_r = \frac{k_i}{z} = \frac{k_i}{p_2} = \frac{p_1}{b_1} \quad (11)$$

Consequently, the current TF can be derived by the designed parameters as:

$$G_{rc}(s) = \frac{b_1 k_r}{s + p_1} = \frac{b_1 k_i}{p_2} \frac{1}{s + p_1} = \frac{p_1}{s + p_1} \quad (12)$$

It means that $G_{rc}(s)$ is reduced to a standard FOS. The settling time of (12) can be approximated by

$$t_{set} = \frac{4}{p_1} \quad (13)$$

For $G_{dc}(s)$, k_d can be chosen as $-b_1/b_2$ which results in $G_{dc}(s) = 0$. This will improve the disturbance-rejection ability.

III. PROPOSED CONTROL OF SC GRID-CONNECTED APPLICATIONS

Figure 1 shows the topology of a grid-connected application for the SC. The SC is connected to the DC bus by a bi-directional DDC that regulates the DC bus voltage, and then the DC bus is connected to the grid via a DC-AC converter. Grid-following or grid-forming control can be adopted for the DC-AC converter. This paper will focus on the control of the DDC.

A. Current Control

Figure 2 shows a detailed DDC with a dual-loop control structure. The inner current controller (CC) implements the current control with the zero-steady-state error, while the voltage controller (VC) adjusts the voltage of the DC link to

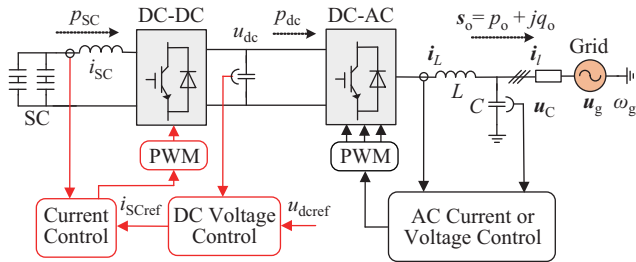


Fig. 1. Grid-connected application for the supercapacitor.

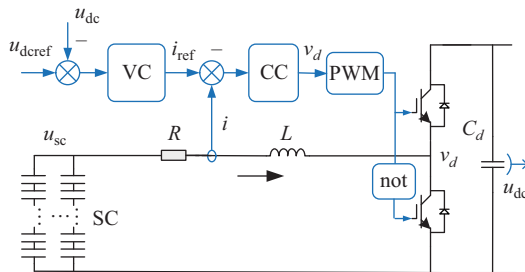


Fig. 2. The control of half-bridge bi-directional DDC.

follow the reference. The switch-average voltage of the bridge middle point v_d is used as the control input to linearize the DDC to model the DDC as a first-order objective. The duty cycle can be computed as $d = v_d/u_{dc}$, which can decouple the effect of the DC bus voltage. In this condition, the inductor current can be modeled in a first-order SS form:

$$\frac{di}{dt} = -\frac{R}{L}i - \frac{1}{L}v_d + \frac{1}{L}u_{sc} \quad (14)$$

with $a = -R/L$, $b_1 = -1/L$, $b_2 = 1/L$, $x_p = i$, and PWM gain K_{PWM} is considered as one. The transfer function (TF) is:

$$G_i(s) = \frac{i}{v_d} = \frac{-1}{sL + R} \quad (15)$$

1) Conventional PI Control

The current control loop acts as the inner loop of the voltage loop; hence, the bandwidth of the current loop should be as high as possible. When the PI controller is used for the current inner loop, a small-signal model of the current loop can be developed, as shown in Fig. 3 [2]. Assuming the PWM is considered as a unity link, the control CL of the current can be expressed as:

$$i = G_{cr}(s)i_{ref} = \frac{k_{pi}s + k_{ii}}{Ls^2 + (R + k_{pi})s + k_{ii}}i_{ref} \quad (16)$$

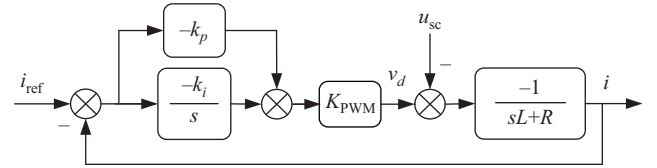


Fig. 3. Small-signal model of the conventional PI control.

The disturbance in the SC voltage can be neglected due to the large capacitance value. As shown in (16), the reference tracking gain $G_{cr}(s)$ is a second-order transfer function (TF) with a zero which is not a classical SOS. Supposing the characteristic equation of the SOS is:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (17)$$

with poles of

$$p = -\zeta\omega_n \pm j\sqrt{1 - \zeta^2} \quad (\zeta < 1) \quad (18)$$

where

$$\zeta\omega_n = \frac{R + k_{pi}}{2L}, \quad \omega_n^2 = \frac{k_{ii}}{L} \quad (19)$$

If the damping factor ζ is 0.707, then, the settling time within 2% of the final value

$$T_{set} = \frac{4.4}{\zeta\omega_n} \quad (20)$$

Apparently, the PI parameters can be designed by (19) with desired T_{set} and ζ . However, for the SOS with a zero, even if the damping factor is designed as a critical value of 0.707, the overshoot is still large, because the zero usually exacerbates oscillation during the dynamic process [26]. For the OVL, this is undesirable.

2) Proposed Control

The suggested approach in Section II is employed to the DC-DC current control to improve the DR of the inner current control, as illustrated in Fig. 4.

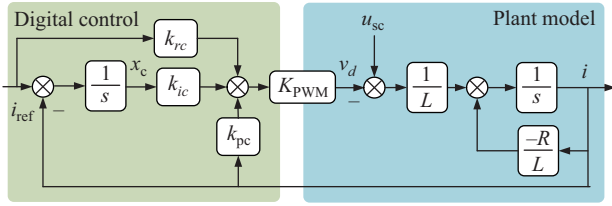


Fig. 4. Proposed SS-based current control.

The control law (4) becomes

$$v_d = k_{pc}i + k_{ic}x_c + k_{rc}i_{ref} \quad (21)$$

where the disturbance gain is omitted because the SC voltage changes slowly. Then according to (10) and (11), the parameters can be computed as:

$$\begin{aligned} k_{pc} &= R + L(p_{1c} + p_{2c}) \\ k_{ic} &= -p_{1c}p_{2c}L \\ k_{rc} &= k_{ic}/p_{2c} = -p_{1c}L \end{aligned} \quad (22)$$

where p_{1c} and p_{2c} are the current loop's CL poles. Consequently, the designed parameters will result in the TF of the current control as:

$$G_{rc}(s) = \frac{i(s)}{i_{ref}(s)} = \frac{p_{1c}}{s + p_{1c}} \quad (23)$$

which means the current inner control will have a superior DR with the characteristics of a FOS. According to (13), the pole p_{1c} can be determined by the desirable settling time, while p_{2c} can be designed smaller to reduce the values of k_{pc} and k_{ic} , as well as the smaller parameters will benefit noise suppression.

B. DC Bus Voltage Control

For the DC bus voltage control, a power-based model of the DC-link is often adopted to achieve a linear model. With the capacitor C_d , the DC bus's power model can also be expressed as a FOS:

$$\frac{1}{2}C_d \frac{du_{dc}^2}{dt} = p_{sc} - p_d \quad (24)$$

with $a = 0$, $b_1 = 2/C_d$, and $b_2 = -2/C_d$, and $x_p = u_{dc}^2$. The disturbance p_d is the output power of the DC bus. The equivalent loss resistor is ignored so the condition of worst damping is considered.

1) Conventional PI Control

Generally, DC bus voltage control also adopts a conventional PI controller. Fig. 5 shows the small-signal control diagram of a conventional PI DC bus control. G_{rc} is the CL of the current control. Generally, the outer loop should have at least one-fifth of the current loop bandwidth. As a result, the inner power stage might be regarded as a unity link. Then CL TF of the DC voltage control is:

$$u_{dc}^2 = G_{vr}(s)u_{dc}^2_{dref} = \frac{2k_{pv}s + 2k_{iv}}{C_d s^2 + 2k_{pv}s + 2k_{iv}}u_{dc}^2_{dref} \quad (25)$$

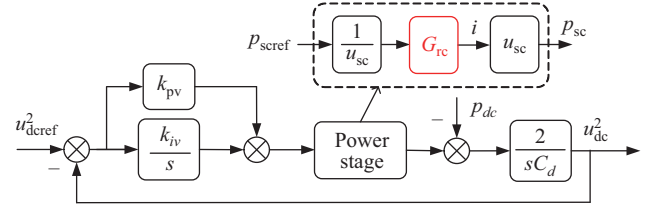


Fig. 5. Control block diagram of the DC-link voltage loop.

Sometimes, a resonant controller is also employed in parallel with the PI controller to address the double-line-frequency ripple (DLFR) at the expense of complicated control implementation [11]. Similar to (16), (25) is also an SOS with a zero. According to the characteristic equation of the SOS (17) and (18), the PI parameters can be designed as:

$$k_{pv} = \zeta\omega_n C_d, \quad k_{iv} = 0.5\omega_n^2 C_d \quad (26)$$

Then the settling time of the voltage loop within 2% of the final value is:

$$T_{set,v} = \frac{4.4}{\zeta\omega_n} = \frac{4.4C_d}{k_{pv}} \quad (27)$$

2) Proposed DC Voltage Control

When the proposed control is employed to the inner current control, the DR of the inductor current can be designed very fast, even lower than 1 ms with zero overshoot within 10–20 kHz switching frequency. Consequently, the dynamic of the current loop can be ignored in the design of the DC voltage control. The proposed control method is first applied to the DC bus voltage control without considering the current loop. The effect of the current loop will be analyzed later.

Figure 6 shows the proposed control method for the DC bus voltage control. The control law is:

$$i_{ref} = \frac{1}{u_{sc}} (k_{pv}u_{dc}^2 + k_{iv}x_{cv} + k_{rv}u_{dc}^2_{dref} + k_d p_d) \quad (28)$$

where x_{cv} is the state variable of the integrator

$$\frac{dx_{cv}}{dt} = u_{dc}^2_{dref} - u_{dc}^2 \quad (29)$$

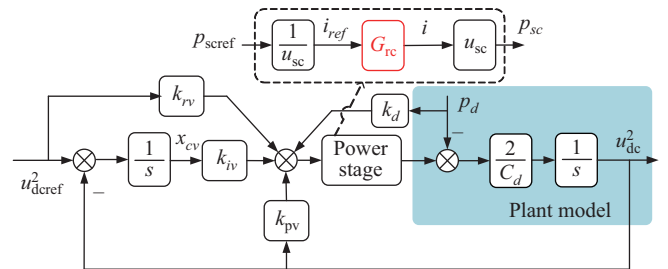


Fig. 6. Proposed simple control for DC bus voltage control.

Using (10) and (11), it has

$$\begin{aligned} k_{pv} &= -0.5C_d(p_{1v} + p_{2v}) \\ k_{iv} &= 0.5C_dp_{1v}p_{2v} \\ k_{rv} &= k_{iv}/p_{2v} = 0.5C_dp_{1v} \end{aligned} \quad (30)$$

Correspondingly, p_{1v} and p_{2v} are the pre-defined CL poles of the DC bus loop. The resulting reference-output TF is:

$$G_{vr}(s) = \frac{u_{dc}^2}{u_{dcref}^2} = \frac{p_{1v}}{s + p_{1v}} \quad (31)$$

If we design $p_{1v} \gg p_{2v}$ which is feasible, the settling time can be approximated as:

$$T_{set,v} = \frac{4}{p_{1v}} \approx -\frac{2C_d}{k_{pv}} \quad (32)$$

Compared with (27), it can be found the same proportional gain can obtain a faster settling speed with the proposed method.

Moreover, the disturbance feedforward is designed as $k_d = -b_1/b_2 = 1$. For a grid-connected application, the disturbance power is the instantaneous active power of the DC-AC converter p_o which is available to implement the feedforward. In this condition, the DLFR is expected to be eliminated due to the high bandwidth of the inner current loop. Nevertheless, for general application, a DC load that is directly connected to the DC bus should be considered. However, the DC power disturbance is generally not measured; hence, a power estimation is needed.

Supposing the DC load changes slowly, which means

$$\frac{dp_d}{dt} = 0 \quad (33)$$

We can design the disturbance observer

$$\frac{d}{dt} \begin{bmatrix} \hat{u}_{dc}^2 \\ \hat{p}_d \end{bmatrix} = \begin{bmatrix} 0 & \frac{-2}{C_d} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{u}_{dc}^2 \\ \hat{p}_d \end{bmatrix} + \begin{bmatrix} \frac{2}{C_d} \\ 0 \end{bmatrix} p_{SC} + \begin{bmatrix} l_1 \\ l_2 \end{bmatrix} (u_{dc}^2 - \hat{u}_{dc}^2) \quad (34)$$

where $[\hat{u}_{dc}^2 \ \hat{p}_d]^T$ are the estimates of $[u_{dc}^2 \ p_d]^T$, and $[l_1 \ l_2]^T$ are observer gains. Defining the error vector as $e = [e_1 \ e_2]^T = [u_{dc}^2 - \hat{u}_{dc}^2 \ p_d - \hat{p}_d]^T$, the dynamic error equations can be derived based on (20), (26) and (27)

$$\frac{d}{dt} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} -l_1 & \frac{-2}{C_d} \\ -l_2 & 0 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \quad (35)$$

Therefore, observer gains can be designed directly by the pole placement.

3) Analysis Including Current Dynamic

Previous DC voltage control design ignores current dynamics to achieve order reduction. To analyze the effect of current dynamics, the SC power dynamic is considered as:

$$\frac{p_{SC}(s)}{p_{SCref}(s)} = G_{rc}(s) = \frac{p_{1c}}{s + p_{1c}} \quad (36)$$

which can be expressed in the SS model

$$\frac{dp_{SC}}{dt} = -p_{1c}p_{SC} + p_{1c}p_{SCref} \quad (37)$$

Combining (20), (23), and (30), the open-loop system is:

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} u_{dc}^2 \\ x_{cv} \\ p_{SC} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 2/C_d \\ -1 & 0 & 0 \\ 0 & 0 & -p_{1c} \end{bmatrix} \begin{bmatrix} u_{dc}^2 \\ x_{cv} \\ p_{SC} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ p_{1c} \end{bmatrix} p_{SCref} \\ &+ \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} u_{dcref}^2 + \begin{bmatrix} -2/C_d \\ 0 \\ 0 \end{bmatrix} p_d \end{aligned} \quad (38)$$

Then the control law (22) can be rewritten as:

$$p_{SCref} = k_{pv}u_{dc}^2 + k_{iv}x_{cv} + k_{rv}u_{dcref}^2 + k_dp_d \quad (39)$$

Substituting (32) into (31), the CL model is obtained as:

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} u_{dc}^2 \\ x_{cv} \\ p_{SC} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 2/C_d \\ -1 & 0 & 0 \\ p_{1c}k_{pv} & p_{1c}k_{iv} & -p_{1c} \end{bmatrix} \begin{bmatrix} u_{dc}^2 \\ x_{cv} \\ p_{SC} \end{bmatrix} \\ &+ \begin{bmatrix} 0 \\ 1 \\ p_{1c}k_{rv} \end{bmatrix} u_{dcref}^2 + \begin{bmatrix} -2/C_d \\ 0 \\ p_{1c}k_d \end{bmatrix} p_d \end{aligned} \quad (40)$$

Using (33), we can verify the effect of the inner current dynamic.

First, two controllers are designed as $p_{1c} = 6200$, $p_{2c} = 50$ and $p_{1c} = 2300$, $p_{2c} = 65$ for the ICL based on the parameters shown in Table I. The resulting gains are $k_{rc} = -11.18 \ \Omega$, $k_{pc} = 11.22 \ \Omega$ and $k_{ic} = 547.72 \ \Omega \cdot s^{-1}$ and $k_{rc} = -4.18 \ \Omega$, $k_{pc} = 4.25 \ \Omega$ and $k_{ic} = 273.85 \ \Omega \cdot s^{-1}$, respectively. The p_{1c} is selected small to achieve small control gains. Settling time of the current within 2% steady state error can be approximated by $4/p_{1c}$. Based on the current loop, the DC bus voltage control is designed to have poles of $p_{1v} = 46$, $p_{2v} = 1$ where p_{2v} is cancelled by the feedforward. The resulting gains are $k_{rv} = 0.1518 \ S$, $k_{pv} = -0.1518 \ S$ and $k_{iv} = 0.1518 \ S \cdot s^{-1}$. The power feedforward is set as $k_d = 1$.

TABLE I
PARAMETERS OF THE TEST SYSTEM

Symbol	Performance	Value
L	Inductance of AC filter	1 mH
C	Capacitance of AC filter	54 μF
R	Inductor resistance	0.05 Ω
L_g	Grid-side inductance	1.5 mH
L_{sc}	SC-side inductance	1.8 mH
SC	Super capacitance	2 F
C_d	DC link capacitance	3300 μF
f_s	Switching frequency	16,000 Hz
	AC Voltage RMS/frequency	120 V/60 Hz

Figure 7 shows the zero-pole locations of the designed DC bus voltage controller. It is verified from Fig. 7 the ICL will not affect the zero-pole cancellation feature of the DC bus voltage loop with the proposed control.

IV. VERIFICATION

An experimental platform with the topology of Fig. 1 is built with a DSP TMS320F28379D (32-bit floating-point) to test the effectiveness of the proposed control method. Table I lists the parameters of the experimental platform. The switching frequency f_s is 16 kHz.

A. Current Control

Figure 8 illustrates the experimental results of the current control with the two designed controllers which are demonstrated in Section III.B.3. A current step from $-10 \ A$ to $0 \ A$ is tested for the two controllers. As shown in Fig. 8(a), when the poles are set as $p_{1c} = 2300$, $p_{2c} = 50$, and $z = 50$, settling time of the inductor current is 1.5 ms which accords with the design of $p_{1c} = 2300$. When p_{1c} is improved to 6200, the

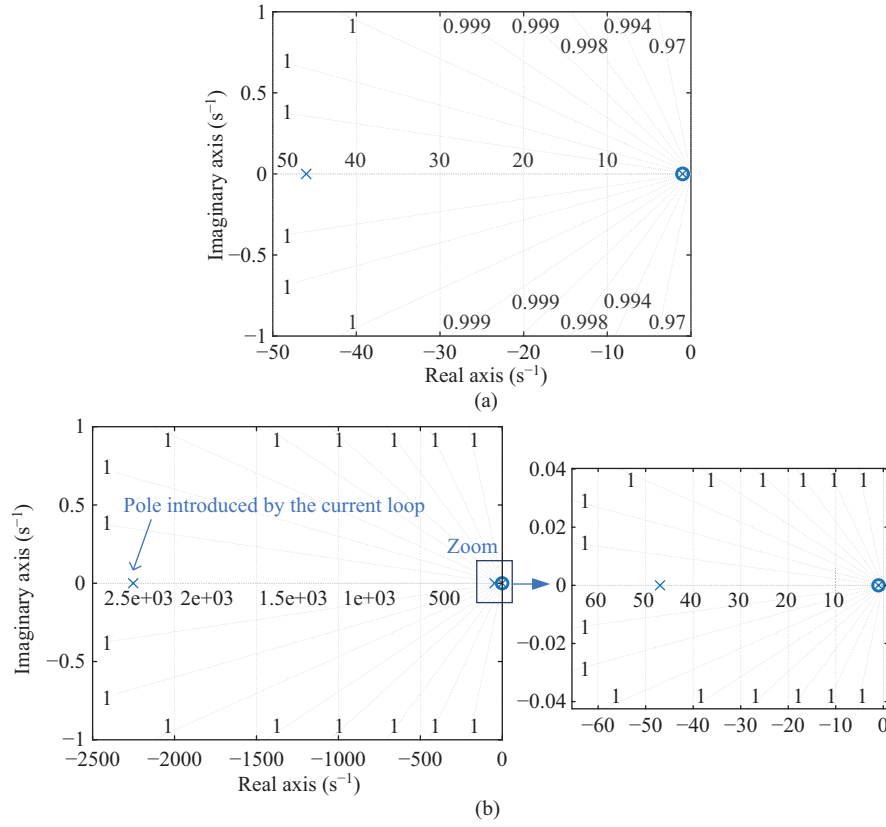


Fig. 7. Zero-pole location of the DC bus voltage control. (a) Ignoring the inner current loop. (b) Considering the ICL with $p_{1c} = 2300$.

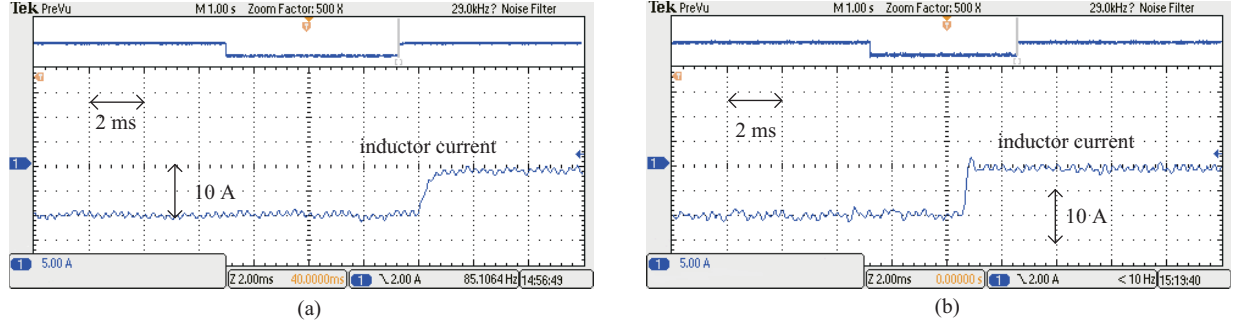


Fig. 8. Step responses of the current control. (a) $p_{1c} = 2300$. (b) $p_{1c} = 6200$.

current waveform exhibits a very fast DR with 0.4 ms settling time and a small overshoot. This performance is beneficial for the outer voltage control.

B. DC Bus Voltage Control

Based on the proposed current control, the designed DC bus voltage control is also designed and tested. The parameters are shown in Section III.B.3. Moreover, conventional PI control is implemented as a comparison. The parameters are $k_{pv} = 0.3137$ S, and $k_{iv} = 7.4578$ S·s $^{-1}$ which leads to 10 Hz bandwidth and damping of 0.707. According to (27), the theoretical settling time is 47 ms.

The reference step response is first tested for the proposed control and the typical PI control. The reference jumps from 400 V to 700 V with a step of 50 V. Fig. 9 shows the comparative results. As shown in Fig. 9(a), the proposed

control method demonstrates an excellent DR with 80 ms settling time and zero overshoot. This settling time accords with the design of $p_{1v} = 46$. In contrast, Fig. 9(b) shows the conventional PI control performs about 200 ms settling time, and the overshoot is large, although the damping is designed as 0.707. The real settling time and overshoot are deteriorated by the unconfigurable zero. Moreover, to compare the overshoot with the same settling time, $p_{1v} = 20$, $p_{2v} = 1$. The experiment result is shown in Fig. 10. It can be seen from Fig. 10 that the overshoot still disappeared when the settling time is about 200 ms.

Furthermore, considering the operation range of the SC voltage is wide, the robustness of the proposed method is also tested with the condition of 150 V and 400 V SC voltage, respectively. Fig. 11 shows the experimental result, which demonstrates good DR of the proposed control method for

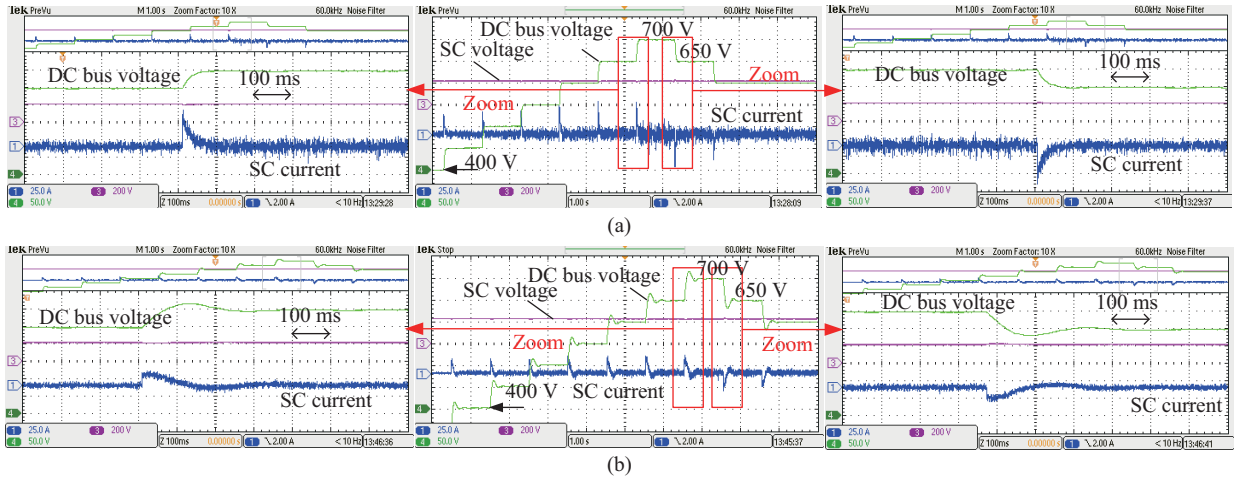


Fig. 9. Step responses of the DC bus voltage control with SC voltage 210 V. (a) Proposed control. (b) Conventional PI control.

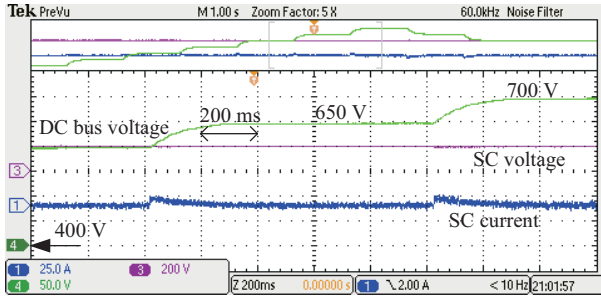


Fig. 10. Step responses of the DC bus voltage with $p_{1v} = 20$, $p_{2v} = 1$.

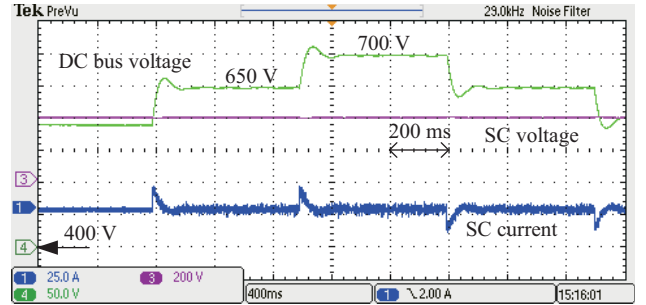
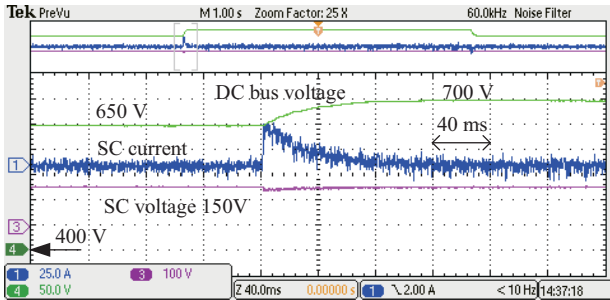
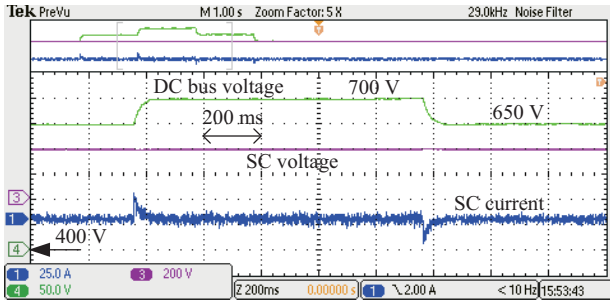


Fig. 12. Step responses of the DC bus voltage for the robust control [20].



(a)



(b)

Fig. 11. Step responses of the DC bus voltage control with SC voltage (a) 150 V and (b) 400 V for the proposed control.

both 150 V and 400 V SC voltage. The settling time is about 80 ms, and the overshoot is absent. Robustness of the proposed control method is good. To further evaluate the performance of

the proposed method, robust control [20] is also implemented as a comparison. As shown in Fig. 12, the robust control [20] still has the overshoot when the reference steps. The reason is the zero still exists for the robust control.

C. DC Load Test

To further verify the disturbance-rejection ability, a DC load step experiment is conducted for three control schemes: (a) a proposed method with the power feedforward; (b) a proposed method without the power feedforward; and (c) a conventional PI control with the power feedforward. DC power is estimated by the observer designed in Section B.2).

Figure 13 shows the experimental results where the estimated current is obtained by $\hat{p}_d/u_{dc}$. The estimated current demonstrates the proposed observer works well, and the load current is successfully estimated. Moreover, comparing Fig. 13(a) with (b) shows that, when load steps, the proposed control method without power feedforward has a slow DR and big voltage drop due to small pole p_{2v} . However, when we use the power feedforward to offset the pole p_{2v} , the DR becomes much better, recovering time is short and the voltage drop is much smaller. In contrast, although a conventional PI controller also adopts power feedforward, recovering time and voltage drop are still large.

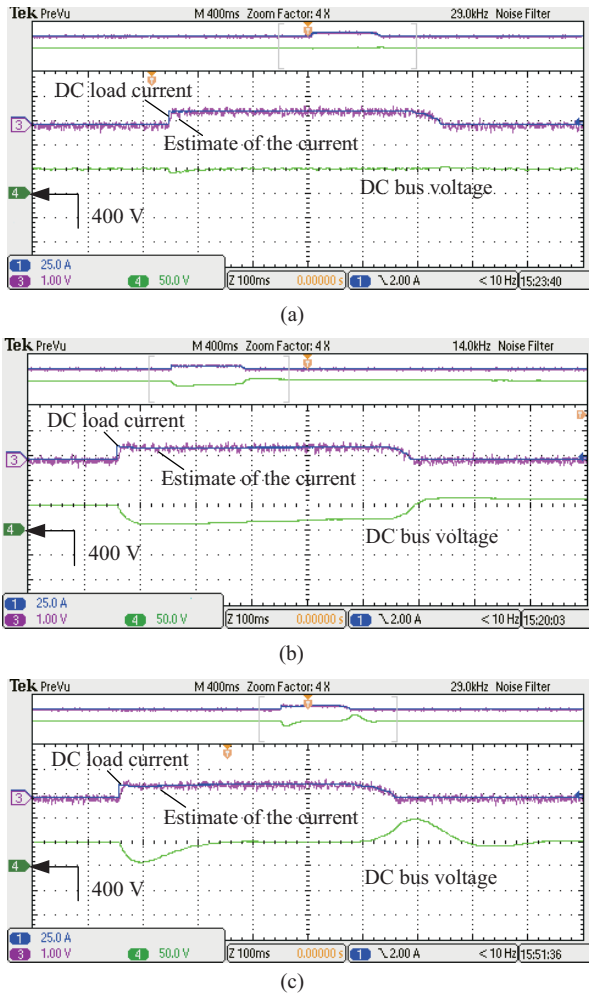


Fig. 13. Performance of DC load step. (a) Proposed method with the power feedforward. (b) Proposed method without the power feedforward. (c) PI control with the power feedforward.

D. DLFR

For grid-connected applications, the issue of the DLFR on the DC bus has to be addressed. When an SC is employed for grid-connected applications, the SC has a natural advantage to address the DLFR because of large capacitance. For the proposed control method, a simple power feedforward control can eliminate the DLFR due to the high bandwidth of the current loop. Fig. 14 shows the DLFR test results. Phase B grid voltage was adjusted to 100 V to generate an unbalanced power. As shown in Fig. 14(a), when the power feedforward is not adopted, the SC output direct current and the DC bus manifested a 15 V amplitude DLFR. The double-line-frequency power is provided by the DC bus capacitor. Nevertheless, as shown in Fig. 14(b), the SC outputs current with the double-line-frequency component when the power feedforward is applied. It means the double-line-frequency power is supplied by the SC but not the DC bus capacitor; consequently, the double-line-frequency voltage ripple is eliminated.

V. CONCLUSION

In this paper, a simple and effective control method is proposed for a SC DC-DC converter (DDC). With the pro-

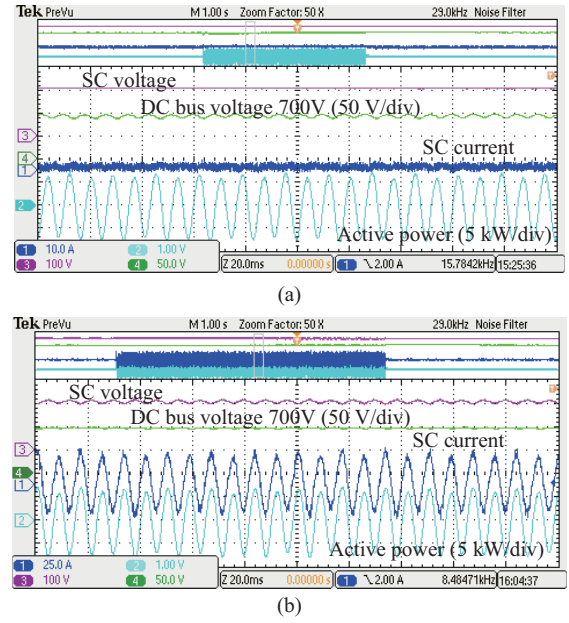


Fig. 14. Performance with unbalanced grid. (a) Without the power feedforward. (b) With the power feedforward.

posed control method, current and voltage control can be reduced to a standard first-order system (FOS); consequently, the dynamic responses of the current and voltage control are improved. High robustness against the SC voltage variation is also achieved. The double-line-frequency ripple (DLFR) is well addressed in grid-connected applications by the proposed simple control method without multiple resonant controllers. Finally, the effectiveness and robustness of the proposed simple control method are verified by experimental results.

In the proposed method, the disturbance voltage of the low-voltage side is considered to be slowly varying, hence the proposed method is suitable for the SC and battery application.

REFERENCES

- [1] U. Manandhar, N. R. Tummuru, S. K. Kollimalla, A. Ukil, G. H. Beng, and K. Chaudhari, "Validation of faster joint control strategy for battery- and supercapacitor-based energy storage system," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3286–3295, Apr. 2018.
- [2] X. J. Quan, R. Y. Yu, X. Zhao, Y. Lei, T. X. Chen, C. J. Li, and A. Q. Huang, "Photovoltaic synchronous generator: architecture and control strategy for a grid-forming PV energy system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 936–948, Jun. 2020.
- [3] X. Dou, J. Wang, Z. Zhang and M. Gao, "Optimal configuration of multitype energy storage for integrated energy systems considering system reserve value," *CSEE Journal of Power and Energy Systems*, vol. 10, no. 5, pp. 2114–2126, Sept. 2024.
- [4] P. J. Grbovic, P. Delarue, P. Le Moigne, and P. Bartholomeus, "Modeling and control of the ultracapacitor-based regenerative controlled electric drives," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3471–3484, Aug. 2011.
- [5] B. Faridpak, M. Farrokhifar, M. Nasiri, A. Alahyari and N. Sadoogi, "Developing a super-lift Luo-converter with integration of buck converters for electric vehicle applications," *CSEE Journal of Power and Energy Systems*, vol. 7, no. 4, pp. 811–820, Jul. 2021.
- [6] S. You, Z. Wang and Y. Sun, "Charging strategy of integrated onboard EV charger with small intermediate capacitor," *CSEE Journal of Power and Energy Systems*, vol. 11, no. 4, pp. 1810–1819, Jul. 2025.

- [7] Q. W. Xu, N. Vafamand, L. L. Chen, T. Dragičević, L. H. Xie, and F. Blaabjerg, "Review on advanced control technologies for bidirectional DC/DC converters in DC microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1205–1221, Apr. 2021.
- [8] X. Liu, T. Zhao, H. Deng, P. Wang, J. Liu and F. Blaabjerg, "Microgrid energy management with energy storage systems: a review," *CSEE Journal of Power and Energy Systems*, vol. 9, no. 2, pp. 483–504, Mar. 2023.
- [9] X. Xie, X. Quan, Z. Wu, X. Cao, X. Dou and Q. Hu, "Adaptive Master-Slave Control Strategy for Medium Voltage DC Distribution Systems Based on a Novel Nonlinear Droop Controller," *IEEE Transactions on Smart Grid*, vol. 12, no. 6, pp. 4765–4777, Nov. 2021.
- [10] L. Wang, Y. Liu, Y. Guo, Q. H. Wu and G. Tang, "Stability analysis of DC-DC converters with energy balance control," *CSEE Journal of Power and Energy Systems*, vol. 9, no. 5, pp. 1765–1773, Sept. 2023.
- [11] M. Mellincovsky, V. Yuhimenko, M. M. Peretz, and A. Kuperman, "Low-frequency DC-link ripple elimination in power converters with reduced capacitance by multiresonant direct voltage regulation," *IEEE Transactions On Industrial Electronics*, vol. 64, no. 3, pp. 2015–2023, Mar. 2017.
- [12] E. Mohammadi, R. Rasoulinezhad, and G. Moschopoulos, "Using a supercapacitor to mitigate battery microcycles due to wind shear and tower shadow effects in wind-diesel microgrids," *IEEE Transactions on Smart Grid*, vol. 11, no. 5, pp. 3677–3689, Sep. 2020.
- [13] B. Talbi, F. Krim, A. Laib, A. Sahli, and A. Krama, "PI-MPC switching control for DC-DC boost converter using an adaptive sliding mode observer," in *Proceedings of 2020 International Conference on Electrical Engineering (ICEE)*, 2020, pp. 1–5.
- [14] O. Andrés-Martínez, A. Flores-Tlacuahuac, O. F. Ruiz-Martínez, and J. C. Mayo-Maldonado, "Nonlinear model predictive stabilization of DC-DC boost converters with constant power loads," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 822–830, Feb. 2021.
- [15] C. Asma, Z. Abdelaziz, and Z. Nadia, "Dual loop control of DC-DC boost converter based cascade sliding mode control," in *Proceedings of 2017 International Conference on Green Energy Conversion Systems (GECS)*, 2017, pp. 1–6.
- [16] Y. Y. Cheng, G. H. Wen, and H. B. Du, "Design of robust discretized sliding mode controller: analysis and application to buck converters," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10672–10681, Dec. 2020.
- [17] C. Olalla, I. Queinnec, R. Leyva, and A. El Aroudi, "Optimal state-feedback control of bilinear DC-DC converters with guaranteed regions of stability," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3868–3880, Oct. 2012.
- [18] S. Kasichyanula and V. John, "Adaptive control strategy for ultracapacitor based bidirectional DC-DC converters," *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1717–1728, Mar./Apr. 2019.
- [19] X. Z. Zhang, Z. Y. Lu, X. F. Yuan, Y. N. Wang, and X. J. Shen, "L2-gain adaptive robust control for hybrid energy storage system in electric vehicles," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 7319–7332, Jun. 2021.
- [20] X. B. Dou, X. J. Quan, F. Chen, Z. J. Wu, and W. Gu, "Robust control of bidirectional DC/DC convert for super capacitor application," *Proceedings of the CSEE*, vol. 38, no. 1, pp. 223–231, Jan. 2018.
- [21] R. Bhosale and V. Agarwal, "Fuzzy logic control of the ultracapacitor interface for enhanced transient response and voltage stability of a DC microgrid," *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 712–720, Jan./Feb. 2019.
- [22] J. J. Duan, Z. H. Yi, D. Shi, C. Lin, X. Lu, and Z. W. Wang, "Reinforcement-learning-based optimal control of hybrid energy storage systems in hybrid AC-DC microgrids," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 9, pp. 5355–5364, Sep. 2019.
- [23] S. Dusmez and A. Khaligh, "Generalized technique of compensating low-frequency component of load current with a parallel bidirectional DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5892–5904, Nov. 2014.
- [24] Y. C. Zhang, J. Jiao, J. Liu, and J. H. Gao, "Direct power control of PWM rectifier with feedforward compensation of DC-Bus voltage ripple under unbalanced grid conditions," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2890–290, May/Jun. 2019.
- [25] S. N. Li, A. T. L. Lee, S. C. Tan, and S. Y. R. Hui, "Plug-and-play voltage ripple mitigator for DC links in hybrid AC-DC power grids with local bus-voltage control," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 687–698, Jan. 2018.
- [26] A. Mutovkin, V. Yuhimenko, M. Mellincovsky, S. Schacham, and A. Kuperman, "Control of direct voltage regulated active DC-link capacitance reduction circuits to allow plug-and-play operation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6527–6537, Aug. 2019.
- [27] J. Lin and G. Weiss, "An indirect approach to control an active capacitor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2898–2906, Sep. 2020.
- [28] J. Lin and G. Weiss, "Plug-and-play control of the virtual infinite capacitor," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1947–1956, Feb. 2020.
- [29] X. B. Dou, X. J. Quan, Z. J. Wu, M. Q. Hu, J. L. Sun, K. Yang, and M. H. Xu, "Improved control strategy for microgrid ultracapacitor energy storage systems," *Energies*, vol. 7, no. 12, pp. 8095–8115, Dec. 2014.
- [30] B. WAYNE BEQUETTE. Process Control: Modeling, Design and Simulation[J]. IEEE Control Systems Magazine, 2006, 26(6): 106–108.



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